Multi-Objective Layout Optimization for Multi-Chip Power Modules considering Electrical Parasitics and Thermal Performance

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***Abstract*—Multi-Chip Power Modules (MCPMs) allow for integration of high power semiconductor devices and control circuitry into one compact package which yields improved reliability and reduced size, cost, and complexity. The layout design process of an MCPM is time consuming and very multidisciplinary, spanning thermal, electrical, and mechanical issues. A software tool is introduced in this paper which allows for a user to draw a 'stick figure' of a desired MCPM layout which is transformed into a multi-objective optimization problem by the tool. After optimization, a user can browse a set of results which form a trade-off curve of approximately Pareto optimal thermal and electrical parasitic layout performance.**

I. INTRODUCTION

Multi-Chip Power Modules (MCPMs) allow for increased reliability and decreased cost, complexity, and size of power electronics systems by the integration of power switching components and control circuitry into one compact package. The design of MCPMs is currently an iterative process conducted manually with relatively few software automation tools to aid in the procedure. Some software tools have been developed which help tie together the multidisciplinary aspects of power electronic module development in terms of calling sets of Finite Element Method (FEM) tools and pooling the data for analysis [1]. The designer is still required to know a large span of disciplines and manipulate the geometry of a module manually in order to achieve results. The designer may use parametric sweeps to gain a feel for the behavior of a system as certain design parameters change, but will need to explore many sweeps in order to gain an intuition of the overall system. Other software tools have attempted to automate module layout, but only consider parasitic inductance and resistance, or no trade-off information is handled by the designer [2], [3].

This paper presents a software tool which attempts to solve many of these problems and focuses on the layout of trace and placement of devices and leads. Fig. 1 shows the overall structure of an MCPM, where trace layout is the pattern formed on the top metal layer of the substrate.

The core framework of the tool is made up of fast and light weight physical models, a 'stick figure' symbolic layout system, and a multi-objective optimization approach. Two fast physical models have been developed in previous works which were designed for use in this tool. The first is a thermal model which can estimate temperature changes of die junction temperatures under variations in trace layout, die location, and die quantity. This is achieved by placing the temperature distributions from each die in superposition rather than resolving the partial differential heat equation again every time the design is changed. The other is an electrical parasitic model which estimates parasitic layout inductance, resistance, and capacitance using closed form frequency dependent equations [4], [5]. The fast physical models allow for the optimizer to evaluate many different solutions to a layout problem in a short time span rather than placing FEM based tools directly in the optimization loop. These models are not driven towards extremely high accuracy, but are more focused on exposing underlying physical trends. The final solutions found by the tool can next be verified using FEM tools.

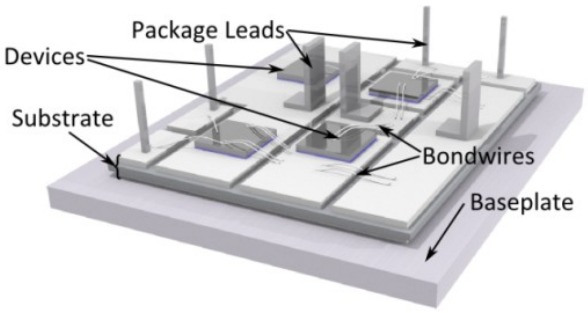

Fig. 1. Typical MCPM power portion (control circuitry usually resides above this structure).

The symbolic layout system allows a designer to quickly draw out a representation of an MCPM layout and next identify design constraints and performance objectives. Since drawing a topology requires very little actual geometric input, this allows the designer to quickly experiment with many layout topologies rather than sticking to one. This symbolic layout is processed by an algorithm which extracts a multi-objective optimization problem from it and attempts to solve for the Pareto optimal trade-off curve with respect to the chosen constraints and performance objectives. For example, if a layout is made more compact in order to reduce parasitic inductance, the high power semiconducting devices will be forced into closer proximity to each other, increasing the temperature of the devices. Thus, there exists a trade-off between thermal and electrical parasitic performance in module designs.

II. Fast Thermal and Electrical Parasitic Modeling

A. *Thermal Modeling*

The fast thermal modeling technique developed for this tool primarily uses spatial superposition of temperature distributions to determine the temperature of devices in a module. The temperature and flux distribution of a device is characterized from a single run of a FEM simulation of a single die in the module. Fig. 2(b) shows a representation of an extracted temperature distribution. Thermal resistance values in a compact thermal model (CTM), shown in Fig. 2(a), are found by placing each device's characterized temperature distribution in a superposition and considering the interaction of each device's heat flux distribution with the current trace layout. The model is able to predict changes in temperature over variation in trace layout and device positioning at a maximum error less than 10% and around 10,000 times faster FEM [4].

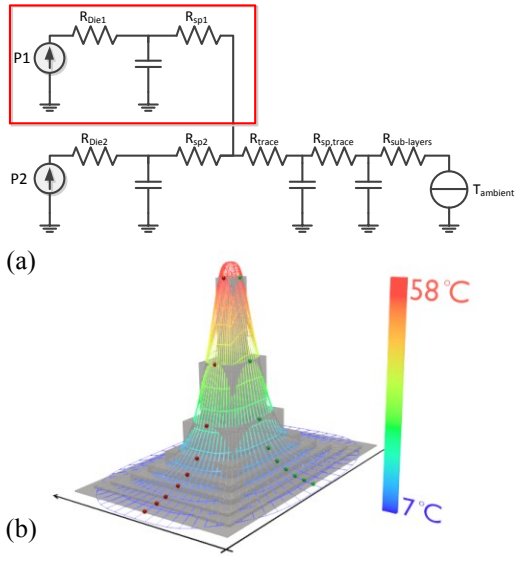

Fig. 2. (a) Structure of CTM with two devices and (b) a characterized distribution for a single device.

B. *Electrical Parasitic Modeling and Extraction*

The electrical parasitics in a module are approximated by closed-form solutions to micro-strip transmission line models. Since power modules share the same basic geometry, as seen in Fig. 3, the micro-strip model equations provide an accurate representation of the parasitic resistance, inductance, and capacitance inherent in power module traces [5]. The micro-strip transmission equations are also frequency dependent which allows for performance estimation at a range of module operating frequencies.

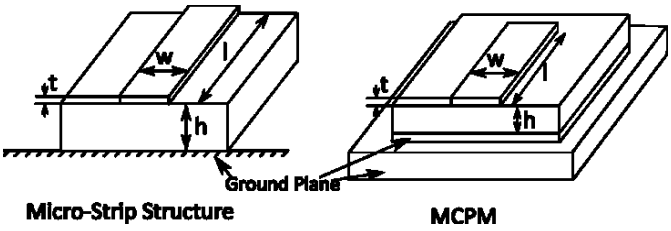

Fig. 3. Comparison between the structure of a micro-strip transmission line and MCPM.

Layouts are automatically broken down into a lumped element network/graph with resistance and inductance values for each element/edge approximated by micro-strip transmission line equations. Fig. 4 shows the nodes and paths which make up the parasitic extracted network. This network is found by traversing each trace segment (green rectangles) and placing nodes at points which connect to other trace segments, devices, leads, or bond wires. The length of each graph edge is measured and the segment trace width is used as input to the micro-strip transmission line equations. The micro-strip transmission line equations also require the thickness and height of the trace above the baseplate which are inputted by the designer and held constant over the optimization process.

Capacitance from trace to baseplate (effective ground-plane) is evaluated at each lumped element node. The trace area around the node is used instead of the segment based approach for the resistance and inductance above.

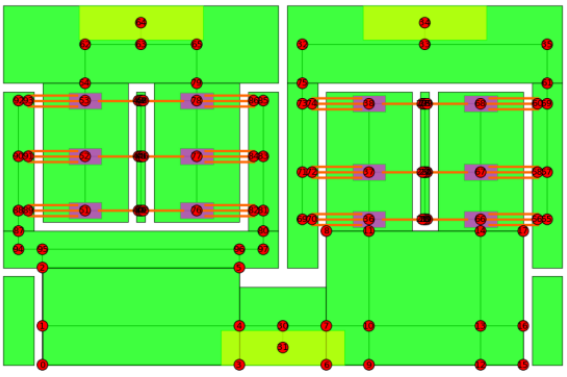

Fig. 4. Parasitc extraction nodes and paths superimposed on a layout.

Once the lumped element network is extracted, the network is transformed into an admittance matrix. The effective

impedance between any two nodes can be determined by placing a unitary flow between the nodes: a source and a sink. After the flows have been placed in a column vector, standard linear algebraic techniques are used to find the potential between the nodes and thus the effective impedance is found.

III. Symbolic Layout Representation

The symbolic layout system is a simple drawing of the topology of an initial module layout. A symbolic layout is comprised of three basic elements: lines, points, and rectangles. The line elements represent traces or bond wires. The point elements represent particular devices or leads, and the rectangle elements represent traces which span multiple traces vertically or horizontally in topological space. A symbolic layout is drawn by a designer in an external scalable vector graphic (SVG) editor and imported into the tool. The symbolic layout is rendered in the tool and is presented to the user as an interactive figure. Fig. 5(a) shows an example of a symbolic layout and Fig. 5(b) shows a corresponding geometric layout.

A designer chooses a set of performance measures, in this case electrical or thermal, by selecting topological points in the symbolic layout. For example, a user can select the top left and top right green points in Fig. 5(a) and add a measure of layout inductance between these two topological points. Electrical measures can be made between any two topological points in a symbolic layout. A user can also select a number of points which represent devices and request the maximum temperature of the group of devices be returned and optimized for.

Geometric constraints can also be added to the problem by selecting line segments in the symbolic layout and either applying a minimum and maximum width of the line segments or a fixed width. The overall size of the layout is assumed to be constrained to a fixed width and length (chosen by the designer).

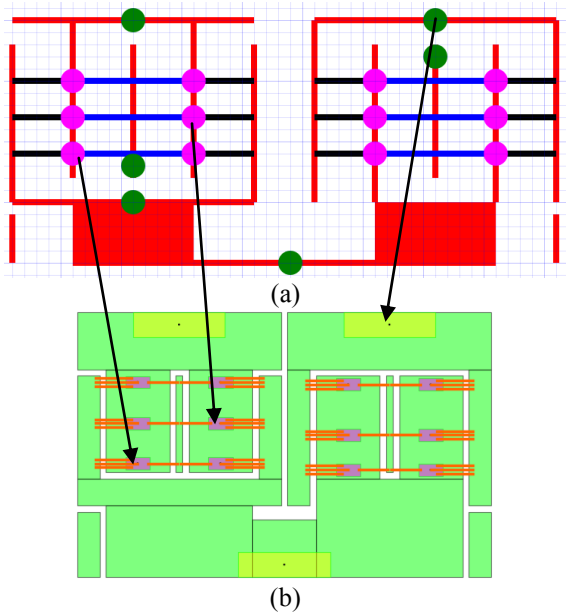

Fig. 5. (a) Symbolic layout of multiple MOSFET half bridge MCPM (b) one representation of the symbolic layout in actual geometry.

IV. Multi-Objective Optimization

A multi-objective optimization problem is formulated based on the symbolic layout by allowing each layout line element some variable width which constitutes a set of design variables. The length of the line segments are determined by the widths of the orthogonal line segments and total width or length of the layout. This set of design variables determines the geometric representation of a symbolic layout. Giving differing values of the design variables yields different geometric outcomes. Thus, the optimizer makes changes to these design variables and evaluates the performance measures specified by the designer. If multiple performance measures are present, the optimizer attempts to find the best trade-off solutions between these performance measures.

The Non-dominated Sorting Genetic Algorithm II (NSGA-II) is used to perform the optimization procedure [6]. This algorithm attempts to find the true Pareto frontier of an optimization problem and also spread out along the front as much as possible yielding the designer a larger ranged design space.

V. Results

An example multi-objective optimization problem was constructed in relation to a preexisting commercial layout. The overall topology of the layout was constructed with three performance measures: maximum device temperature, loop inductance and loop resistance. The loop inductance and resistance are the measure of the path between the top left lead and top right lead, weaving through the entire layout.

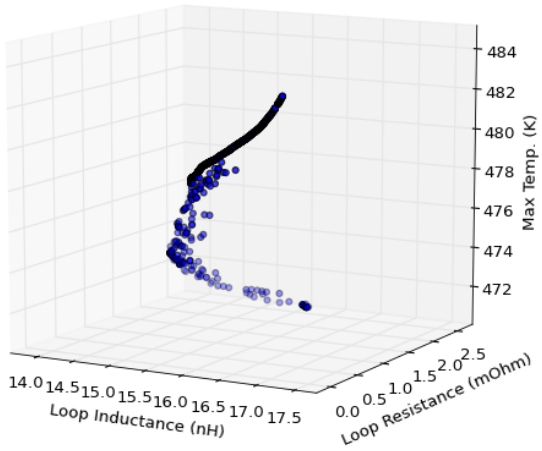

Fig. 6. Pareto frontier of the example design problem.

Fig. 6 shows the resultant Pareto front after running NSGA-II for 1500 generations which ran in 300 s on a single threaded process on an Intel Core i7 clocked at 2.93 GHz. The front is represented in a three dimensional space reflecting the three performance objectives targeted in this problem. The front follows a primarily one dimensional curve in space which is due to the correlation between loop resistance and loop inductance. Each point in the front represents a unique layout solution. The graph shown in Fig. 6 is actually an interactive graph where a designer can select

different solutions from the front and quickly evaluate the design space.

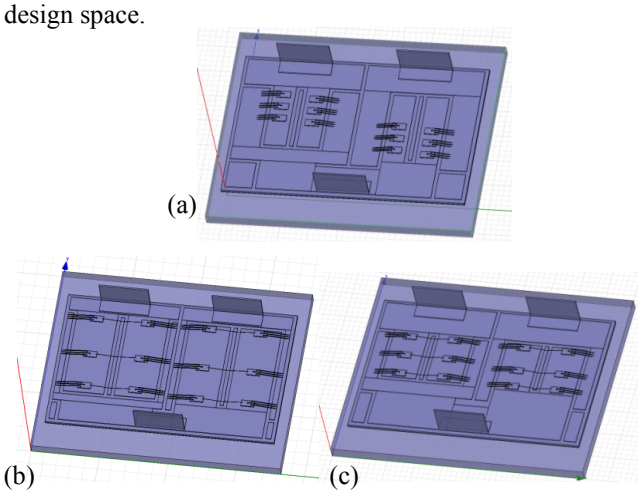

Fig. 7. (a) A commercial layout solution, (b) Layout 1 solution selected from Pareto front, and (c) Layout 2 solution selected from Pareto front.

Two layout solutions chosen from the Pareto front in Fig. 6 are shown in Fig. 7(b) and (c). The layout shown in Fig. 7(a) is a commercially designed layout. Layout 2 chosen from the front decreases the loop inductance, resistance, and the maximum (top surface average) device temperature over the Commercial layout; see Table I for numerical detail. Layout 1 decreases the maximum temperature in the module by about 5 °C, but fails to reduce the loop inductance and resistance with respect to the Commercial layout. As can be seen in Layout 1, the devices have spread out away from each other and thus increased the length of the traces surrounding traces. This process has lowered the temperature, but increased layout parasitics.

TABLE I. SELECTED MULTI-OBJECTIVE LAYOUT SOLUTIONS VS. COMMERCIAL LAYOUT

		Loop Ind. (nH)	Loop Res. (mΩ)	Max. Temp. (K)	Max. Avg. Temp. (K)
Commercial	*FEM*	12.69	1.1	477	476.23
Layout 1	*Fast Model*	15.89	1.67	-	471.55
	FEM	13.34	1.282	471.8	470.95
Layout 2	*Fast Model*	14.8	1.19	-	473.8
	FEM	12.05	0.969	474.4	473.57

VI. CONCLUSIONS AND FUTURE WORK

A set of approximately optimal trade-off solutions for power module layouts can easily be found for a power module layout allowing a designer easy access to the full design space of a layout topology. This system also allows a designer to quickly test many different layout topologies while maintaining layout quality. The fast electrical and thermal models both predict temperature and parasitic values accurately with respect to FEM tools. By decreasing the design process time significantly, this tool reduces cost associated with multi-chip power modules. In future work, the entire layout process could be automated by using a genetic algorithm. Due to the discrete nature of the symbolic layout system, it would be possible to build up a set of layout topologies instead of a user performing this task. Next, this set of layout topologies would be passed to the multi-objective optimizer and a user could select from a broader design space. Other physical models could also be incorporated into the optimization system. Further research will be conducted into gauging thermal stress and electromagnetic interference (EMI). EMI is a large cause of concern for power module designers and can lead a module to catastrophically fail. Finding better layout topologies which ease EMI problems would greatly benefit this area.

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